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Irradiation of VFAT3 A 128-channel charge-sensitive front-end chip for the CMS GEM phase-2 upgrade

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Abstract

– gt AbstractVFAT3 is the 128-channel charge-sensitive front-end chip explicitly designed for the CMS GEM phase-2 upgrades. LHC is undergoing major high luminosity upgrades for HL-LHC where the particle rate is expected to increase up to 5 times. It is therefore necessary to monitor the evolution of the VFAT3 response due to aging in the radiation environment by total ionizing dose (TID) tests. The device operation could also be interrupted by a single high-energy particle. Thus, the estimation of the single event upset (SEU) cross-section is essential as well. This contribution summarizes all the irradiation test results that validate the suitability of VFAT3 for CMS GEM phase-2 upgrades.– gt SummaryThe VFAT3 is a 128-channel charge readout ASIC specifically designed for CMS GEM detector charge readout. Two different radiation characterization campaigns were launched to qualify the chip for CMS operation TID and SEU tests. TID tests have been conducted at the CERN microelectronics X-ray facility, and VFAT3 was irradiated with a monochromatic beam of X-rays at 1.8 Mrad/hr for several hours of beam time. The chip response was measured for possible variation in its internal parameters. VFAT3 was exposed up to 70 Mrad of TID with a mono-energetic X-ray beam and showed excellent robustness to the radiation. No significant deterioration is observed in the core device functionality during the test. However, the I/O block of the chip showed sensitivity towards the TID. A frequent communication break was observed after 35 Mrad of TID. In CMS, the GEM detectors would receive a maximum of 1 Mrad of TID in the HL-LHC. The TID results show that neither aging nor communication performance degradation is expected to disturb VFAT3 operation in CMS GEMs.The SEU tests were performed at Louvain-La-Neuve heavy-ion facility (HIF). The ions of varying stopping powers were used to irradiate the VFAT3, and corresponding upsets in the device registers were recorded. The SEU cross-sections and extrapolations to the HL-LHC conditions are also established. The VFAT3 registers are triplicated and showed low statistics of bit-flips (saturation cross-section 6.1 X10$^{-}10cm2/bit), agoodindicationoftherobustnessofthedeviceagainstSEUeffects.Acommunicationbreakdownissuei$
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$LHC.ThisfrequencyiswellbelowCMSglobalresetrequestfrequencyforthemuonstations.TheresultsshowthatVFAT3$

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Irradiation of VFAT3: A 128-channel charge-sensitive front-end device for the CMS GEM phase-2 upgrade

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ABSTRACT: VFAT3 is a 128-channel charge-sensitive front-end ASIC explicitly designed for the CMS GEM phase-2 upgrades. LHC is undergoing major upgrades for HL-LHC, where the particle rate is expected to increase up to 5 times. It is, therefore, necessary to monitor the evolution of the VFAT3 response due to aging in the radiation environment by total ionizing dose (TID) tests. The device operation could also be interrupted by a single high-energy particle. Thus, the estimation of the single event upset (SEU) cross-section is essential as well. We summarize irradiation test results that validate the suitability of VFAT3 for CMS GEM upgrades.

KEYWORDS: Radiation damage to electronic components, Radiation-hard electronics

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Contents

1 Introduction

VFAT3 is a front-end ASIC explicitly designed for the readout of Gas Electron Multiplier (GEM) detectors for the phase-2 upgrade of the CMS experiment [1]. The CMS Muon collaboration is incorporating three different Gas Electron Multiplier (GEM) stations to enhance the muon trigger and tracking capabilities. These GEM stations, namely GE1/1, GE2/1, and ME0, will use VFAT3 as a common front-end. GEM detectors will receive up to 1-Mrad of TID for 10 HL-LHC years. VFAT3 must tolerate both the cumulative and single event effects during operation. We performed both total ionizing dose (TID) and Single Event Upset (SEU) tests of the device to find its radiation tolerance and suitability for CMS GEM operation.

The device consists of 128 analog channels composed of a charge-sensitive amplifier, a shaping network, and a constant fraction discriminator. A dedicated calibration, bias, and monitoring (CBM) block is embedded in the device to configure the analog front-end. A block diagram of the VFAT3 ASIC is shown in Figure 1.

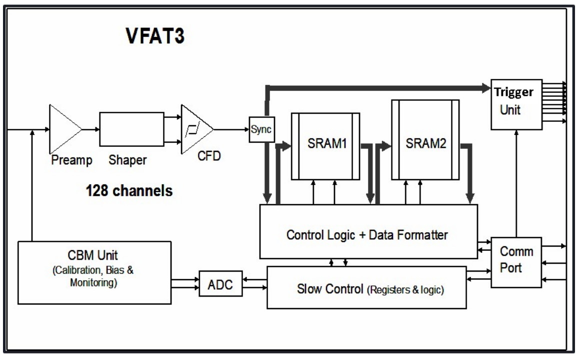
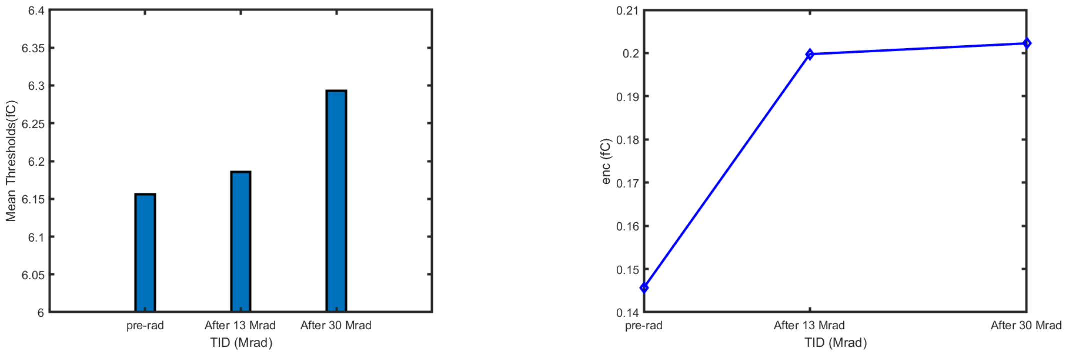


Figure 1: Simplified VFAT3 block diagram

The VFAT3 front-end channels process fast GEM-like signals and produce a binary digital pulse at the CFD output. A "sync" block then splits the signal into two parallel paths, "trigger" and "tracking". The trigger path feeds to a trigger unit which transmits trigger data for every bunch crossing with a fixed latency. The tracking path contains 2 SRAM memories, control logic, and a data formatter. The first SRAM (128 x 1024) is used for storing all channel information at every bunch crossing until receipt of a level-1 trigger. Triggered information is then passed to SRAM2 (176 x 512) as well as corresponding time tags. The data formatter then assembles data packets for transmission at 320Mbps through a serial communication port.

2 VFAT3 TID measurements

VFAT3 TID testing is performed at the CERN X-Ray facility, named ObeliX [2]. Two independent test campaigns were done at dose rates of 1.84 and 5.5 Mrad/hr. The first test was conducted to evaluate the radiation effect on the internal blocks of the device. The second test was conducted to investigate some communication issues encountered during the first test. The global threshold and mean noise measurements for all channels are two key parameters that represent device performance. The TID effect on the mean threshold and Equivalent Noise Charge (ENC) was recorded and shown in Figure 2.

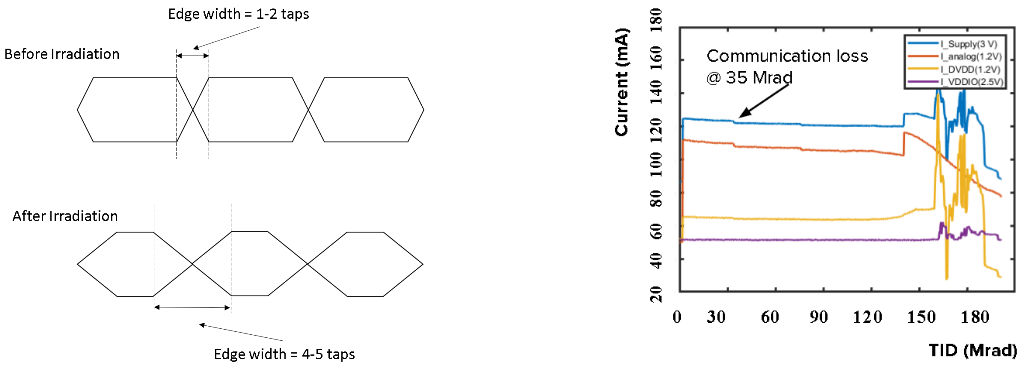


(a) TID effect on mean thresholds of all channels

(b) TID effect on mean ENC (fC) of all channels

Figure 2: VFAT3 front-end channel threshold and noise (ENC) variation after TID

The mean threshold increased by 0.07% after 1 Mrad of TID. The ENC increased by 1.3% after 1 Mrad. At 35 Mrad, the VFAT3 chip stopped communication with the external FPGA, and neither the hard reset nor power cycling succeeded in recovering the communication. Of two devices irradiated, one recovered after 60 hours of room temperature annealing whilst the other showed permanent damage. A second TID campaign (@5.5Mrad/hr) was launched to investigate the communication issue. Both VFAT3 power domains (digital, analog, and I/O) and communication links were monitored throughout the test. The VFAT3 uses Scalable Low Voltage Signaling (SLVS). The e-link is composed of 3 differential SLVS pairs running at 320MHz. The three pairs are Clock, DataIn and DataOut when seen from the VFAT3 side. The phase margin of DataOut eye for the TXD line was reduced linearly with TID up to 35 Mrad, and then a permanent communication was lost. The phase margin reduction is shown in Figure 3a, which may be related to an increase in threshold voltage mismatch and a rise of leakage current of I/O transistors in the VFAT3 device.



(a) VFAT3 data-line phase margin reduction after TID.

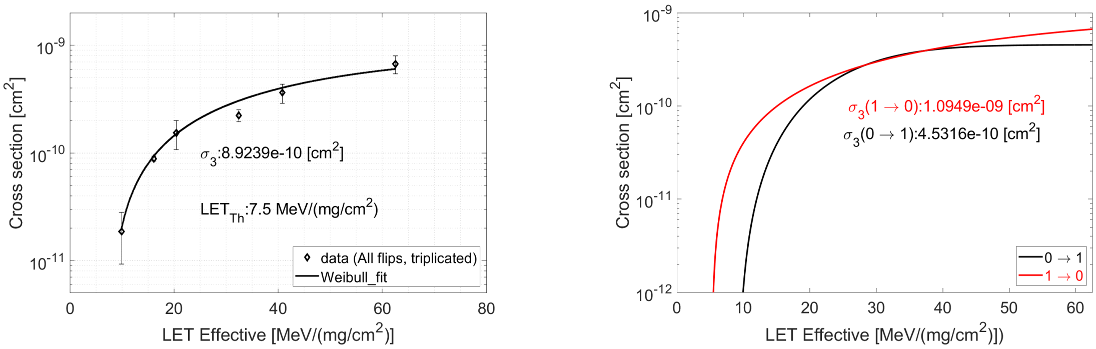
(b) VFAT3 Current variation versus TID (Mrad)

Figure 3: VFAT3 synchronization loss investigation.

The power monitoring for all three domains during the TID also showed a small glitch at 35 Mrad confirming damage to the device, as shown in Figure 3b.

3 VFAT3 single event upset test

The VFAT3 SEU test has been conducted at the Cyclotron Resource Centre (CRC) of Louvain-La-Neuve (LLN), Belgium, in a Heavy Ion Facility (HIF). A VFAT3 configuration registers SEU test was performed to observe bitflips. A saturation cross-section and threshold LET (Linear energy transfer) were calculated. A cross-section plot for VFAT3, taking into account all the bit-flips transitions, is shown in Figure 4a. A comparison of individual $0 \to 1$ and $1 \to 0$ cross-sections is also shown in Figure 4b. The $0 \to 1$ cross-section is smallest of all three, and $1 \to 0$ cross-section is largest among all cross-sections.



(a) VFAT3 triplicated registers cross-section (per-bit) plot.

(b) VFAT3 register cross-section comparison for $0 \to 1$ and $1 \to 0$.

Figure 4: VFAT3 configuration registers cross-sections for all bit-flips, $0 \to 1$ and $1 \to 0$

The average minimum distances between VFAT3 triplicated register cells, namely A, B, and C were also computed. The minimum value was around 5.6μm for BC cells, as shown in Figure 5.

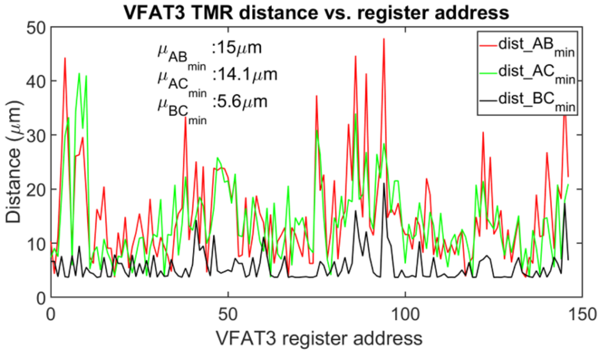


Figure 5: VFAT3 TMR minimum register distance versus register address.

This reduced TMR distance might be the reason behind a small number of flips seen for triplicated registers.

4 VFAT3 synchronization loss (SEFI effect)

The Single Effect Functional Interrupt (SEFI) is defined as a soft error that causes the device to reset, freeze or malfunction in a detectable way. During the VFAT3 heavy-ion beam test, a frequent synchronization loss (SEFI) was observed. The VFAT3 SLVS is a current source-sink block that cannot be triplicated due to manufacturing limitations. A possible functional interrupt at a sensitive node of this SLVS block may be the reason for the observed SEFI. The VFAT3 SEFI cross-section is 2.44 X 10^{-6} cm^2/device as shown in Figure 6.

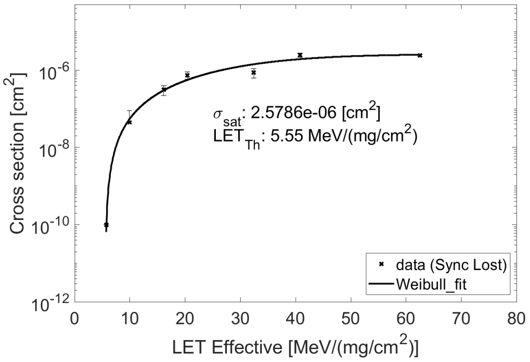


Figure 6: VFAT3 synchronization lost cross-section (per-device)

The extrapolation to HL-LHC conditions is calculated by a computational method to estimate SEU rates in the LHC environment, first introduced by F.Faccio [3]. A convolution of the saturation cross-section at threshold LET of 5.55 MeV/(mg/cm^2), extracted from Weibull fit and the simulated energy deposition probabilities for the proton of different energies (obtained from simulations by the computational method) was done. The SEU cross section in LHC environment can be written as $\sigma_{LHC} = \Sigma_i(P_i \Delta\sigma_i \frac{\sigma_0}{A})$, where for each energy bin i, P_i, the simulated energy deposition probability from the method [3] is also computed. The increase of sensitive area from the Weibull distribution in the same energy bin is $\Delta\sigma_i = (\sigma_{i+1} - \sigma_i)/\sigma_0$. Using the sync lost cross-section Weibull parameters from Figure 6, the equivalent 20 MeV proton cross-section (from computational method) is $\sigma_{LHC} = 6 \times 10^{-14}[cm^2/Device]$. The peak fluxes for GE1/1, GE2/1 and ME0 extracted from FLUKA simulations are $2.04 \times 10^4[Hz/cm^2]$, $9.7 \times 10^3[Hz/cm^2]$, and $3.87 \times 10^5[Hz/cm^2]$ respectively. The sync-lost rate per device in three GEM stations are calculated by multiplying these hadron peak fluxes with σ_{LHC}. Both GE/1 and GE2/1 consists of 3456 VFAT3 devices, and ME0 consists of 5184 VFAT3 devices. The expected sync lost rate, taken in account both endcaps are tabulated (see table 1) as follows:

Detector	Minimum Time between Consecutive sync losses
GE1/1	65.6 hrs
GE2/1	138 hrs
ME0	2.3 hrs

Table 1: VFAT3 sync_loss extrapolation to HL-LHC environment

The HL-LHC extrapolation shows that the VFAT3 synchronization lost phenomenon has very low cross-sections for all three GEM stations. Only the ME0 region indicates a relatively larger cross-section, leading to 1 VFAT3 synchronization loss in the system every 2.3 hours of operation.

5 Summary

In HL-LHC, GEMs would receive up to 1 Mrad of TID, including ME0 stations which would receive maximum hadron flux of 378 kHz/cm^2 in the forward region. The robustness of the VFAT3 ASIC to TID and SEU effects has been studied. During TID tests, less than 1% increase in the channel threshold and 1.3% increase in the ENC has been observed after 1 Mrad of TID (equivalent to 10 HL-LHC years GEM radiation exposure). During the SEU testing of VFAT3 ASIC, the digital register upsets and corresponding saturation cross-sections were computed. The VFAT3 registers showed a small saturation cross-section of 8.9 X 10^{-10} cm^2/bit, which is a good indication of the robustness of the ASIC against the SEU effects. The VFAT3 chip performs well beyond the most severe radiation environment experienced by the CMS GEM detectors and therefore satisfies the CMS GEM radiation requirements for the HL-LHC.

Acknowledgments

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